Demo: Nano Power Draw in Duty-Cycled Wireless Sensor Networks

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ABSTRACT

In this work we present a novel power management architecture for Wireless Sensor Network devices towards minimizing the power consumption when nodes remain in sleep state. Specifically, we propose the employment of an onboard timer circuit that consumes only few nano Amperes, along with a power switch that controls the power rail of the under consideration node. According to our principle, the node remains solely disconnected from power when in sleep state in an effort to minimize the quiescent draw, while the timer is responsible for reinforcing the node back in active mode when required. Our implementation achieves the minimization of power draw in sleep state down to 33 nA, while it can easily be integrated with any IoT platform.

KEYWORDS

Wireless Sensor Networks, Energy Efficiency, Power Consumption Monitoring

1 INTRODUCTION

The unprecedented penetration of Internet-of-Things (IoT) concept in our every day lives, brings numerous interesting applications that attract the attention of the research community. One major area that the community focuses on, is energy efficiency, which is directly associated with network's lifetime. The majority of battery-powered wireless sensor network applications follow a duty-cycle approach, which

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Device	Sleep Principle		
TelosB [2]	5.1 µA	integrated watchdog timer	
Micaz [3]	15 µA	integrated watchdog timer	
Opal [4]	40 µA	integrated RTC	
Waspmote [5]	860 nA	on-board RTC & power switch	
eZ430-RF2500 [6]	690 nA	integrated watchdog timer	
current implementation	33 nA	on-board timer & power switch	

Table 1: Current draw in sleep-state

dictates that the motes switch to sleep state after finalizing a sensing cycle and remain there until the next one.

To implement this technique an interrupt signal is required to awake the host microcontroller back to active state. Commonly, the host microcontroller integrates timer circuits, such as a Real-Time-Clock (RTC) or a Watchdog that are configured to provide the appropriate wake-up signal. Following this principle, the host microcontroller enters in a low-power state, in order to maintain the timing circuit active. Typical sensing applications employ a duty-cycle of 0.1 to 1 % [1], which suggests that the amount of time remaining in sleep state is much longer than the active, thus it is very important to minimize the power consumption even in sleep-state. Table 1 illustrates the power draw of some indicative platforms in sleep state. Notably, most devices exceed 1 μ A in sleep state, while Waspmote and eZ430 are remarkable exceptions, featuring ultra-low power in sleep mode. In this work we present a novel architecture that delivers the outstanding draw of 33 nano Amperes in sleep-state.

2 SYSTEM IMPLEMENTATION

Our implementation is composed of a timer circuit and a power switch. The aforementioned elements can be integrated into the PCB of an available mote or even to be interfaced as an external circuit. We configure the timer to provide a one-shot high output signal after a specified interval through which we control the power switch which in turn powers the under consideration mote. At the time the mote enters its active state it runs all the predefined tasks, such as measure attached probes, process acquired data and propagate frames over the radio. When all tasks

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(b) Proposed architecture w/ timer circuit



(c) Current draw under different rails

Figure 1: NanoIcarus mote along with the Proposed Architecture and Current Consumption Measurements

are completed and the data are stored safely, the mote signals the timer circuit to reboot, thus the timer instantly cuts the power from the mote and countdowns again until the next interval. NanoICARUS mote (Fig. 1(a)) implements the proposed circuitry relying on the ATmega328p, while featuring a XBee-footprint radio socket. Below we present the components used.

Timer: The timer we selected to use is the Texas Instruments (TI) TPL5111 which provides selectable timing intervals from 100 ms to 7200 s. The TPL5111 has a unique one-shot feature where the timer asserts its output pulse for one cycle. We exploit this feature to provide power to the host mote, while we reboot the function of the timer when the mote completes its tasks by signaling its DONE pin, as illustrated in Fig. 1(b) through an I/O pin of the host mote. Moreover, the timer features wide voltage supply range from 1.8 V to 5.5 V, thus the proposed architecture can be easily integrated with all prototypes or commercial motes, just by utilizing one I/O pin for the provision of the *reboot* signal.

Power Switch: In our implementation we evaluated two different power switches that feature ultra-low quiescent current. The TI TPS22860 and the Analog Devices ADG821. Both can drive loads up to 200 mA, while they feature ultrafast response times.

For this implementation it is worth presenting the elapsed wake up time that various MCUs require to wake using internal timers, versus the time they need for a cold start boot. Considering state-of-the-art microcontrollers we chose the mode with the lowest possible consumption with a running internal timer and measured their power consumption in that mode, as well as the time they require to enter an active state when starting cold. As presented in Table 2, MCUs wake up from their various sleep states much faster than starting cold. This difference is less pronounced in some MCUs than others. The trade off for this boost in wake up speed however, is the greatly increased power consumption.

3 **DEMONSTRATION**

To demonstrate the performance of our system we measure the power draw under various voltage levels, and plot the

Mote	Wake-up	Sleep power	Cold start
MSP430FR5969 (LPM 3.5)	291 µs	250 nA	758.4 μs
MSP430F2274 (LPM 3)	16 µs	600 nA	< 100 µs
ATmega328P	110.4 µs	415 nA	61.4 ms
ATmega1284P	5.7908 ms	457 nA	67.5 ms
PIC12LF1552	3.376 ms	220 nA	65.27 ms

Table 2: Wake-Up times of indicative microcontrollers

results in Fig. 1(c). We observe that the TPS22860 switch presents higher draw in higher voltage rails than the ADG821. By comparing the achieved current draw of our implementation in 3.3 V with the eZ430 (Table 1) we observe a reduction of 95.2 %, which can clearly impact on the network's lifetime. To demonstrate the obtained results we utilize the uCurrent meter [7], which is designed to measure ultra-low currents with a resolution of up to 10 pA. Moreover, we employ our monitoring tools [8, 9] to measure the current draw as well as the wake-up times of the various micro-controllers.

4 **CONCLUSIONS**

In this work we presented the nanoICARUS mote that features the outstanding quiescent current of 33 nA, the lowest obtained among all available prototype or commercial motes.

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