Demo: Nano Power Draw in Duty-Cycled Wireless Sensor Networks

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ABSTRACT

In this work we present a novel power management architecture for Wireless Sensor Network devices towards minimizing the power consumption when nodes remain in sleep state. Specifically, we propose the employment of an on-board timer circuit that consumes only few nano Amperes, along with a power switch that controls the power rail of the under consideration node. According to our principle, the node remains solely disconnected from power when in sleep state in an effort to minimize the quiescent draw, while the timer is responsible for reinforcing the node back in active mode when required. Our implementation achieves the minimization of power draw in sleep state down to 33 nA, while it can easily be integrated with any IoT platform.

KEYWORDS

Wireless Sensor Networks, Energy Efficiency, Power Consumption Monitoring

1 INTRODUCTION

The unprecedented penetration of Internet-of-Things (IoT) concept in our every day lives, brings numerous interesting applications that attract the attention of the research community. One major area that the community focuses on, is energy efficiency, which is directly associated with network's lifetime. The majority of battery-powered wireless sensor network applications follow a duty-cycle approach, which dictates that the motes switch to sleep state after finalizing a sensing cycle and remain there until the next one.

Device	Sleep	Principle
TelosB [2]	5.1 μA	integrated watchdog timer
Micaz [3]	15 μA	integrated watchdog timer
Opal [4]	40 μA	integrated RTC
Waspmote [5]	860 nA	on-board RTC & power switch
eZ430-RF2500 [6]	690 nA	integrated watchdog timer
current implementation	33 nA	on-board timer & power switch

Table 1: Current draw in sleep-state

To implement this technique an interrupt signal is required to awake the host microcontroller back to active state. Commonly, the host microcontroller integrates timer circuits, such as a Real-Time-Clock (RTC) or a Watchdog that are configured to provide the appropriate wake-up signal. Following this principle, the host microcontroller enters in a low-power state, in order to maintain the timing circuit active. Typical sensing applications employ a duty-cycle of 0.1 to 1 % [1], which suggests that the amount of time remaining in sleep state is much longer than the active, thus it is very important to minimize the power consumption even in sleep-state. Table 1 illustrates the power draw of some indicative platforms in sleep state. Notably, most devices exceed 1 μA in sleep state, while Waspmote and eZ430 are remarkable exceptions, featuring ultra-low power in sleep mode. In this work we present a novel architecture that delivers the outstanding draw of 33 nano Amperes in sleep-state.

2 SYSTEM IMPLEMENTATION

Our implementation is composed of a timer circuit and a power switch. The aforementioned elements can be integrated into the PCB of an available mote or even to be interfaced as an external circuit. We configure the timer to provide a one-shot high output signal after a specified interval through which we control the power switch which in turn powers the under consideration mote. At the time the mote enters its active state it runs all the predefined tasks, such as measure attached probes, process acquired data and propagate frames over the radio. When all tasks

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